Referring now to FIG. 4, an annealing step has taken place to cause metal 31 (of FIG. 3) to react with active areas 22 and conductors 23 and 25. Conductors 23 and 25 have previously been formed from conductively doped polysilicon. This reaction forms silicide 41 on the surfaces of active areas 22 and conductors 23 and 25. Because the silicide is formed by annealing and is self aligned to the exposed surfaces of active areas 22 and conductors 23 and 25, the newly formed silicide surfaces will now be referred to as salicide surfaces 41. The unreacted metal is then etched away leaving the salicide surfaces 41 shown in the wafer profile illustrated in FIG. 4.

Referring now to FIG. 5, a conformal layer of dielectric 51, such as oxide or nitride is deposited, preferably by CVD. Dielectric 51 is then patterned and etched to provide interconnect (contact) openings to salicide surfaces 41. It is from this point on that the inventive features of the present invention come into play.

Referring now to FIG. 6*a*, a conformal layer of polysilicon 61 is deposited, thus making physical contact to salicide surfaces 41. Although not required, it is preferred to perform a dilute hydrofluoric acid (HF) dip to ensure the salicide surfaces 41 are clean prior to the deposition of polysilicon 61. Next, polysilicon is heavily doped by implanting an impurity such as Arsenic (As) or Phosphorus (Phos) at a sufficient energy to penetrate the interface between polysilicon 61 and salicide surfaces 41, yet not so high of an energy as to effect the final depths of source/drain regions 22.

As an example of the implant step, the inset graph of FIG. 6*b*, illustrates an appropriate dopant concentration of As and the implant energy used with a given polysilicon thickness to accomplish a low resistive contact between polysilicon 61 and the underlying conductive materials via salicided surfaces 41. As shown in this figure, an As concentration of approximately 5×10^{19} atoms /cm^3 is formed in a polysilicon layer being approximately 1000Å thick, by implanting As at an energy of approximately 180 keV with a dose of approximately 5×10^{15} atoms/cm^2. As the profile in this figure shows, salicide 41 bonds strongly with polysilicon by virtue of ion-mixing that occurs during the implant and yet the depth of source/drain region 22 is affected very little. If the use of polysilicon 61 requires a uniformly doped polysilicon, an additional lower energy implant may be performed. This lower level implant will depend on the thickness of the polysilicon used and subsequent anneals in a given process. In addition, to attain the desired doping profile, the implants may be masked depending on the use of the upper level polysilicon (e.g., PMOS thin film transistors or intrinsic resistors where lower doped regions are also required in the upper level polysilicon, thereby necessitating the masking off of those low doped areas from the high dose As implant).

Referring now to FIG. 7, polysilicon 61 is patterned and etched to form the appropriate conductive patterns while preserving low resistive buried contacts. In the preferred embodiment, due to the use of As as the dopant impurity, active areas 22 and polysilicon 25 were previously doped to an n-type conductivity. However, the inventive concept follows by using the appropriate dopant if p-type conductivity were desired.

These low resistive salicide contacts to upper level polysilicon can be implemented into any CMOS fabrication wherever a conductively doped lower level material can be subjected to saliciding techniques. The present invention has been used to create low resistive contacts in memory semiconductor devices such as static random access memory (SRAM) devices.

It is to be understood that although the present invention has been described with reference to a preferred embodiment, various modifications, known to those skilled in the art, may be made to the structures and process steps presented herein without departing from the invention as recited in the several claims appended hereto.

We claim:

1. A process for forming low resistance interconnects between an active area having a silicided surface, and an upper level polysilicon layer, in a process used for fabrication of a semiconductor device on a silicon wafer substrate, said process comprising:

a) forming said active area into said wafer substrate;

b) forming said silicided surface from a layer of metal deposited on said active area;

c) forming a dielectric over existing materials residing over said wafer surface;

d) providing openings to said silicided surface at interconnect locations;

e) depositing a layer of said upper level polysilicon on said dielectric and into said openings to thereby form said silicided surface; and

f) implanting a dopant impurity of arsenic at a dose of approximately 5×10^{15} atoms/cm^2 at an implanting energy of approximately 180 keV into said upper level polysilicon layer being approximately 1000Å thick, thereby conductively doping said layer of upper level polysilicon;

wherein a major portion of implanted conductive impurities reside at the interface between said upper level polysilicon and said silicided surface, thereby forming low resistive contacts between said silicide surfaced active areas and said conductively doped upper level polysilicon.

2. A process as recited in claim 1, wherein said active area forms an n-type source/drain region of an NMOS transistor.

3. A process as recited in claim 1, wherein said active area forms a p-type source/drain region of a PMOS transistor.

4. A process as recited in claim 1, wherein said semiconductor device is a memory semiconductor device.

5. A process as recited in claim 4, wherein said memory semiconductor device is an SRAM.

6. A process as recited in claim 1, wherein said metal is selected from the group consisting of titanium, cobalt, platinum, tungsten, molybdenum, palladium and tantalum.

7. A process for forming low resistance interconnects between a lower level conductively doped polysilicon having a silicided surface, and an upper level polysilicon layer, in a process used for fabrication of a semiconductor device on a silicon wafer substrate, said process comprising:

a) forming said silicided surface from a layer of metal deposited on said lower level conductively doped polysilicon;

b) forming a dielectric over existing materials residing over said wafer surface;

c) providing openings to said silicided surface at interconnect locations;

d) depositing a layer of said upper level polysilicon on said dielectric and into said openings to thereby form said silicided surface; and